

**In the Specification:**

Page 3, paragraph beginning with line 5, please replace with the following amended paragraph:

A sense operation principle in the toggle MRAM is the same as a sense operational principle in the conventional and typical MRAM. That is, the sense operation is carried out by detecting a tunnel current passing through the tunnel film 105 provided between the first free layer 104 and the reference layer 106. If the first free layer magnetization direction is in the parallel state to a reference layer magnetization direction belonging to the reference layer 106, the tunnel current is increased in comparison with the anti-parallel state, which means a magnetoresistance (MTJ resistance) is decreased. Information stored in the memory cell is read out by utilizing this characteristic. For convenience of explanation, it is defined as "1" if the magnetoresistance has a high resistance value Rmax (tunnel current min.) (Fig. 1 [[5]]), and it is defined as "0" if the magnetoresistance has a low resistance value Rmin (tunnel current max.) (Fig. 2).

Page 29, line 17, please replace with the following amended line:

([[8]] 10) Step S10

Page 37, first two paragraphs, please replace with the following amended paragraphs:

If it is assumed that a low resistance case is "0" and a high resistance case as "1", the read-out result (the sense result) should be "0" under  $R_{ref\ (1st)} < R_{ref\ (2nd)}$  (Step S[[0]] 26:

yes). That is, the original data of the selected reference cell 14rs (before the write operation in Step S[[0]] 24) can be read out as "0". However, data of the selected reference cell 14rs is "1" at Step S27.

#### (8) Step S28

The read-out result (the sense result) should be "1" under Rref (1st) > Rref (2nd) (Step S[[0]] 26: no). That is, the original data of the selected reference cell 14rs (before the write operation in Step S[[0]] 24) can be read out as "1". However, data of the selected reference cell 14rs is "0" at Step S28.

Page 46, last paragraph, please replace with the following paragraph:

The second resistance - voltage converter 31b is composed of a grounded-gate amplifier circuit including a transistor 41b, a load 42b and an adding unit 49b. In the transistor 41b, a gate receives the bias voltage Vb, a drain is connected to the load 42b and a source is connected to the main reference bit line 28. The bias voltage Vb functions so as not to apply the voltage equal to or larger than the breakdown voltage of the MTJ (magnetic tunneling junction element 25r) to the source of the transistor 41b, that is, the main reference bit line 28. One of terminals of the load 42b is connected to the voltage source VC and the other terminal thereof is connected to the drain of the transistor 41b. The adding unit 49b is connected to a drain, a wiring supplying a negative offset voltage -Voff and the [[second]] third switch unit 43b. The constant voltage VC is divided by the resistance value Rref of the magnetic tunneling junction element 25r of the reference cell 14r and the load 42b in the first read-out operation (the sense operation) so as to provide  $V_{ref2} = k \cdot R_{ref} - V_{off}$  by adding an offset voltage -Voff to a voltage  $V_{ref} (=k \cdot R_{ref})$  proportional to the resistance value Rref. The  $V_{ref}$  is a voltage on a drain side of the transistor 41b.

Page 47, first full paragraph starting at line 10, please replace with the following amended paragraph:

The second storage unit 32b includes a third switch unit 43b and a capacitor 44b. One of terminals of the third switch unit 43b is connected to the adding unit 49b and the other terminal thereof is connected to one of terminals of capacitor 44b. One/off timing of the third switch unit 43b is controlled by the control signal  $\varphi_1$ . One of terminals of the capacitor 44b is connected to the other terminal of the [[first]] third switch unit 43b, and the other terminal thereof is connected to a terminal on an input side of an inverter 46b. An electrical charge corresponding to Vref2 which is supplied to the [[first]] third switch unit 43b in the first read-out operation (the sense operation) is accumulated in the capacitor 44b so as to store the Vref2.

Page 53, last paragraph, please replace with the following amended paragraph:

If the state is toggled from the initial state of "0" to "1", Vref (1st) and Vref (2nd) are supposed to be Vref (1st) < Vref (2nd) (Step S48: yes). Accordingly, the output signals Q1 and Q2 are made to be in "0" level. On the contrary, if the state is toggled from initial state of "1" to "0", Vref (1st) and Vref (2nd) are supposed to be Vref (1st) > Vref (2nd) (Step S[[06]] 48: no). Accordingly, the output signals Q1 and Q2 are made to be in "1" level.

Page 57, first and second paragraphs, please replace with the following amended paragraphs:

The first determination unit 33a of the second sense amplifier 3 outputs the signal Q1 which indicates the magnitude relation between the resistance values Rref1 (1st) and Rref1 (2nd). The second determination unit 33b outputs the signal Q2 which indicates the magnitude relation between the resistance values Rref2 (1st) and Rref2 (2nd). The determination circuit 48a

determines whether or not the signal Q1 is consistent with the signal Q2. If the signal Q1 is consistent with the signal Q2 (Step S66: yes), the first toggle operation has been normally executed, thereby the process goes on to Step S48. If the signal Q1 is not consistent with the signal Q2 (Step S66: no), the first toggle operation has not been normally executed, thereby the process goes on to Step S[[47]] 67.

(7) Step S67

Because the first toggle operation has not been executed normally, the write current  $I_{WL}$  and the write current  $I_{BL}$  are increased by a predetermined amount so as to start from Step S[[42]] 62 again.